INTENTO DESIGN

INFORMED DECISION MAKING FOR ANALOG

INTENTO DESIGN, INNOVATION FOR ANALOG

TECHNOLOGY BEHIND THE SOLUTIONS

June 2023 - Presentation under NDA

Intento Design Mission

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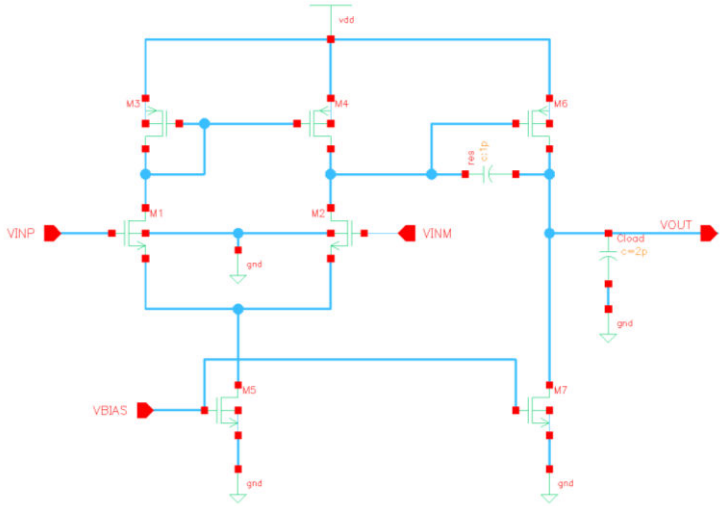
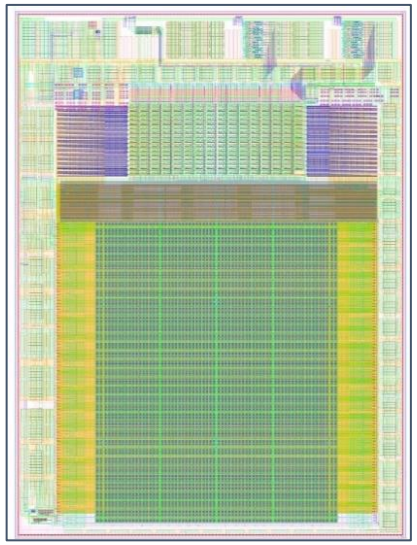
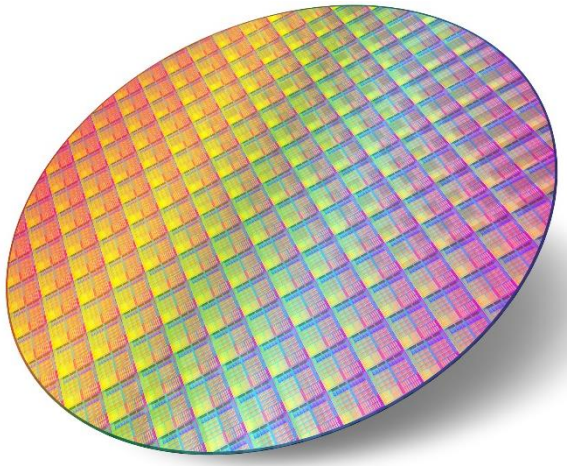
We are a Software company developing Electronic Design Automation tools to design Semiconductor Analog Integrated Circuits



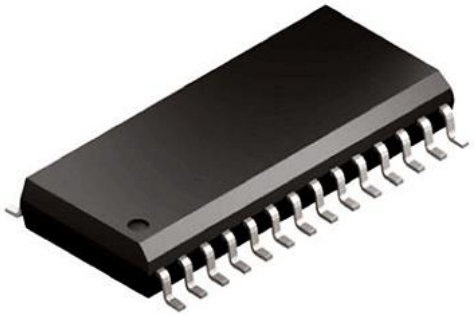
Electrical Schematic



IC Layout



Silicon Wafer



Integrated Circuits

Analog Design Challenges

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Our World is Analog

- Analog circuits are used for
  - Power Management
  - Battery Management
  - Communication (transceiver)
  - Audio
  - Sensors
- Analog Designs are technology dependent
  - They need to be redesigned for every process/foundries
- Analog design flow is still time consuming and laborious with drastic impact cost and time to market.

We need innovation in EDA for Analog

- Analog Designers are becoming rare
  - Hiring is tough
  - Learning curve is long
- Demand for Analog is booming due to
  - Electric vehicles, Battery based systems
  - Modern SoC integrates more and more Analog blocks (Transceiver, DAC, PLL, Interfaces, …)
- Getting an optimum design is costly
  - Time, Human and hardware resources
- Analog Design must support a very large number of silicon technologies and foundries
  - Design porting cost increasing particularly for advanced node
  - First prototyping request is very costly
  - Zero respin is the target

Why do we need innovation in EDA for Analog IC ?

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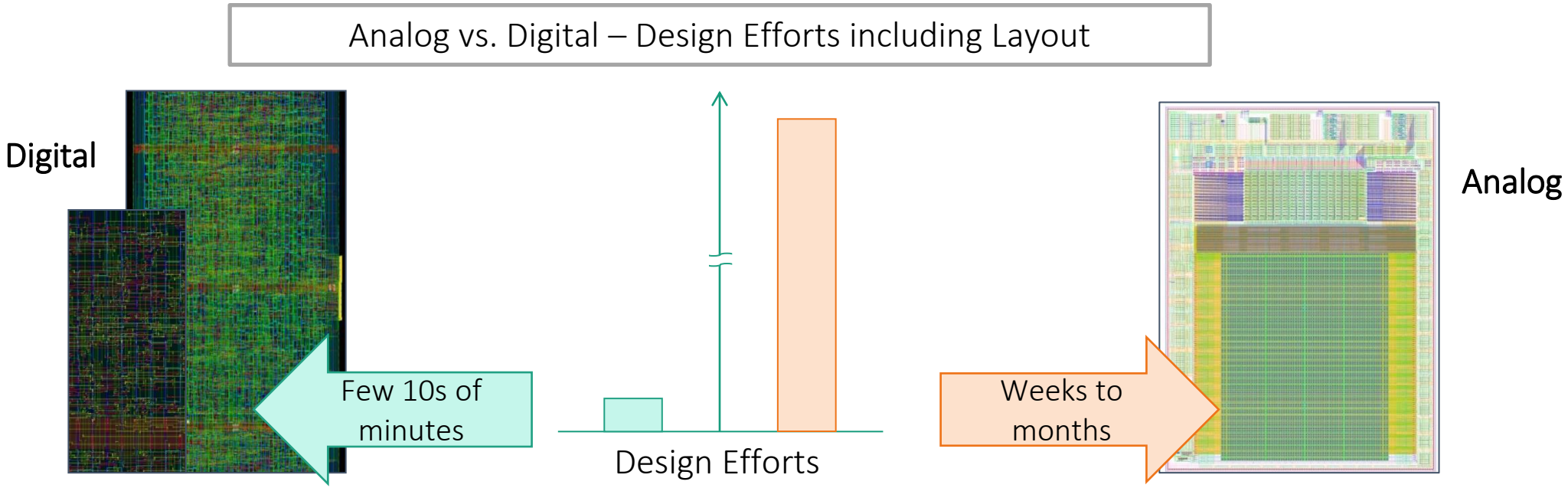
Analog ICs are everywhere around us

- Mobile Phone:
  - Battery Management and Charge
  - Audio, Sensors
- Electric Vehicles:
  - Key components for the Battery Management and Control impacting the range of the vehicle, the speed of charging
- IOT: Sensors, Interfaces,…

Challenges of Analog Design

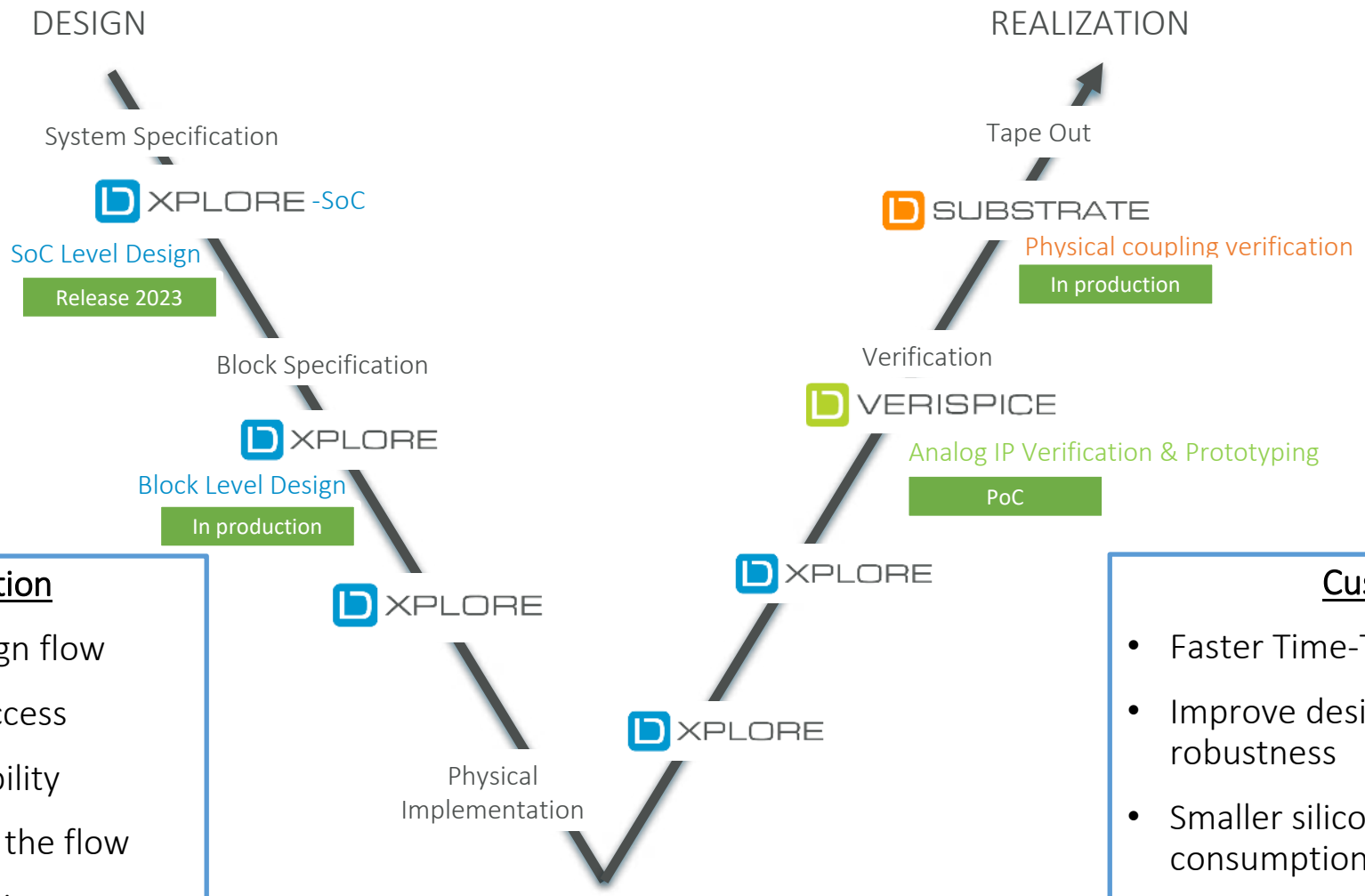
- Analog Designers are becoming rare
- Demand for **Analog is booming**
- Getting an **optimum design is costly**
- Analog Design must support a very **large number of silicon technologies and foundries**
- Need **Efficient Automation** in Analog Design

Motivation to Automate Analog IC Design



- **Business needs:**
  - Improve development cycle time
  - Minimize design errors
  - Reduce Costs
- **Technical pains:**
  - Technologies have a strong impact on Analog
  - Analog design still very “manual”
  - Analog modeling is not mature

Intento Design Solutions for Analog Design Flow



Value Proposition

- Acceleration of design flow
- First-time silicon success
- Maximize chip reliability
- Bring automation in the flow
- Shorten simulation time

Customer Benefits

- Faster Time-To-Market @ reduced cost
- Improve design performance & robustness
- Smaller silicon area & power consumption
- Minimized redesign

Intento Design EDA solutions in Production

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ID XPLORE

- ID-Xplore is a powerful and disruptive EDA tool that can significantly accelerate the design flow.
  - **Easy-to-use**
  - **Fast** and **reliable** design
  - Full integration in design flow with **Virtuoso Environment**
  - Foundry & technology **agnostic**

ID SUBSTRATE

- ID-Substrate captures all types of substrate noise coupling and analyze possible substrate failure effects
  - **Unique** on the market
  - Save **time** and **cost** avoiding reworking
  - Increase **reliability**
  - Full integration in design flow with **Virtuoso Environment**

Already in Production with WW analog leaders like STMicroelectronics, AMS OSRAM and others

In Production

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ID-Xplore™

Ultra Fast Design and Migration of Analog IP

Spice Simulators are based on Nonlinear DC Analysis

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1. From **NR algorithm**: $\boldsymbol{J^k\ \Delta v^k = -f(\ v^k)}$
2. From **LU Decomposition**: $\boldsymbol{J \equiv L\ U} \equiv \begin{bmatrix} J_{11}^{(0)} & 0 & 0 & 0 \\ J_{21}^{(0)} & J_{22}^{(1)} & 0 & 0 \\ J_{31}^{(0)} & J_{32}^{(1)} & J_{33}^{(2)} & 0 \\ J_{41}^{(0)} & J_{42}^{(1)} & J_{43}^{(2)} & J_{44}^{(3)} \end{bmatrix} \begin{bmatrix} 1 & J_{12}^{(1)} & J_{13}^{(1)} & J_{14}^{(1)} \\ 0 & 1 & J_{23}^{(2)} & J_{24}^{(2)} \\ 0 & 0 & 1 & J_{34}^{(3)} \\ 0 & 0 & 0 & 1 \end{bmatrix}$
3. We get: $\boldsymbol{L^k\ U^k\ \Delta v^k = -f(\ v^k)}$
4. Substituting by $\boldsymbol{x^k}$: $\boldsymbol{x^k = U^k\ \Delta v^k}$
5. We first solve the lower triangular matrix by **Forward Substitution**: $\boldsymbol{L^k\ x^k = -f(\ v^k)}$
6. Solve the upper triangular matrix by Back Substitution to get $\Delta \boldsymbol{v}$: $\boldsymbol{U^k\ \Delta v^k\ = x^k}$
7. 7.Finally, we update current variables: $\boldsymbol{v^{k+1} = v^k + \Delta v^k}$

Why Spice Simulations Are Limited in Speed ?

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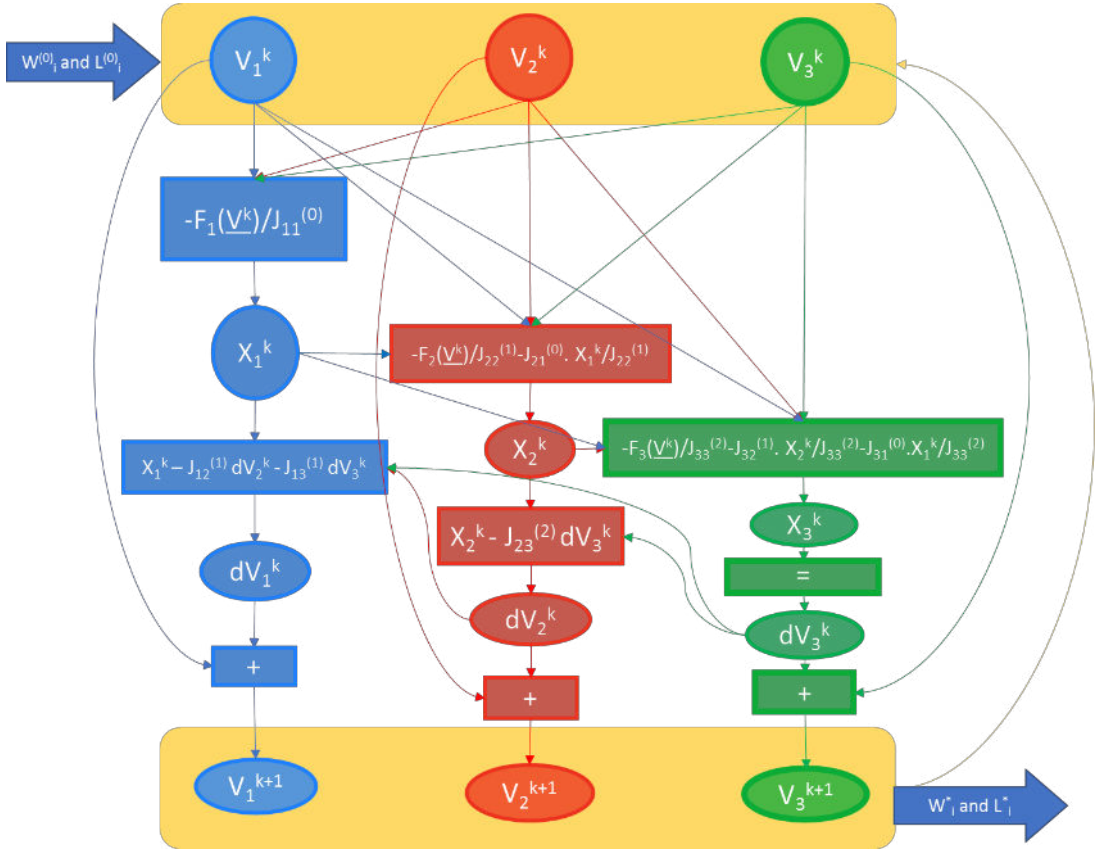
SPICE computational model is complex

- Matrix-based formulation
- Simultaneous Resolution in SPICE:
- Each iteration requires a large number of computations
- Jacobian computation becomes a major difficulty

Representation of Spice DC Simulation



ID-Xplore Approach for Analog Design

Mimic Designer Method for Schematic Design, Migration and Simulation

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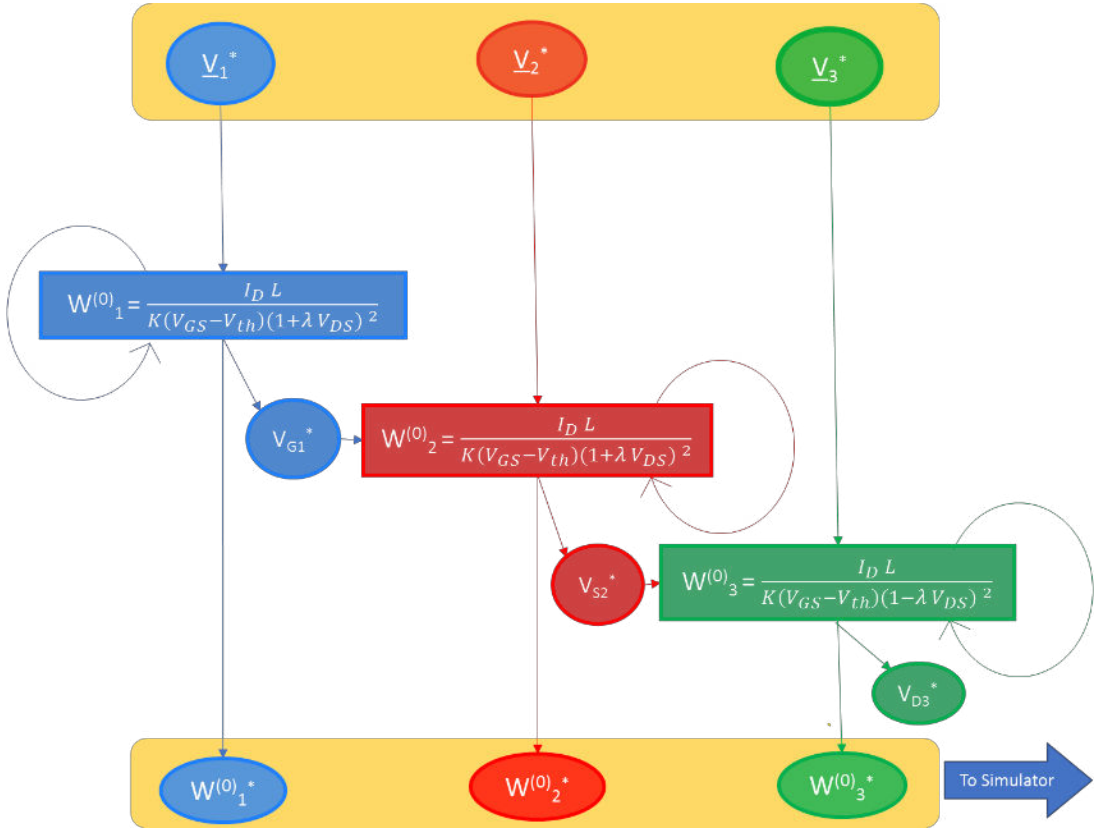
Computational model becomes very simple

- Structured Resolution
- No matrix-based formulation
- Each iteration requires only one computation
- Jacobian computation almost disappears



ID-Xplore Approach for Analog Design:
Digitally EDA-Inspired, Constraint-Driven Design Methodology

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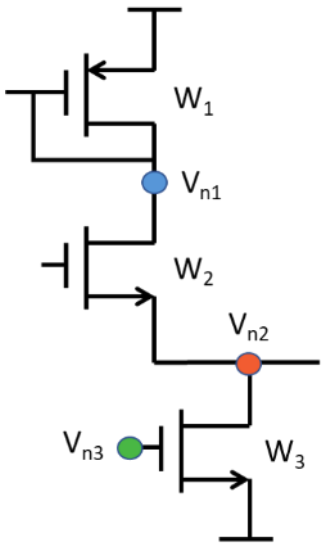

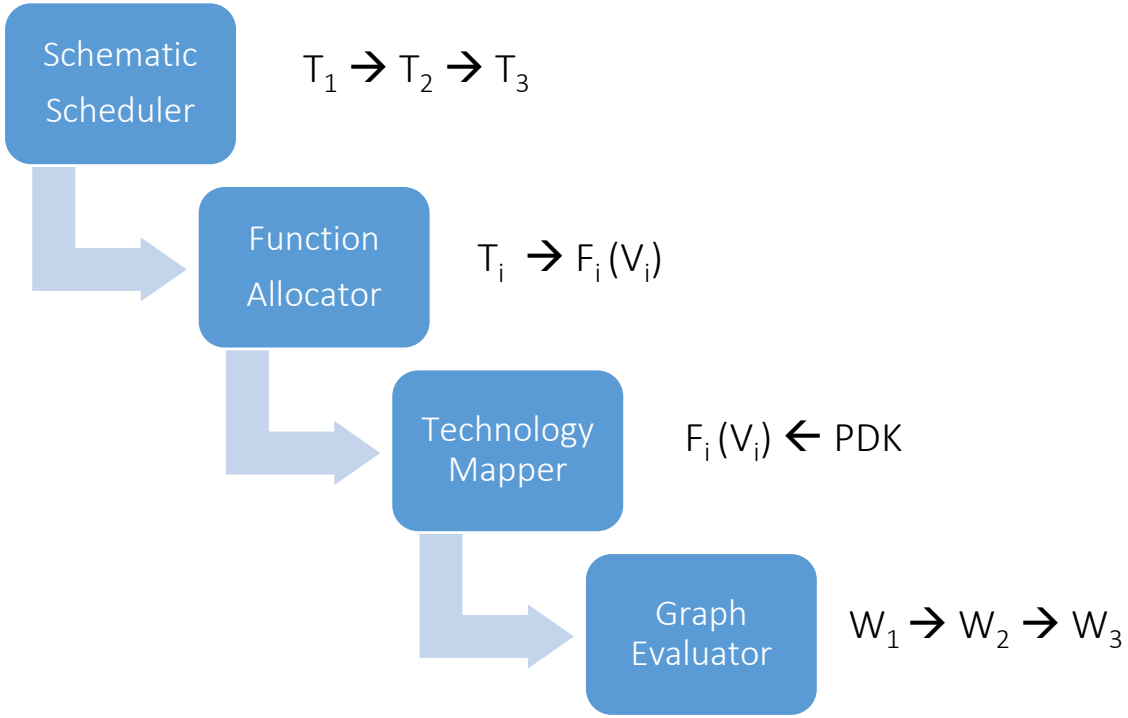

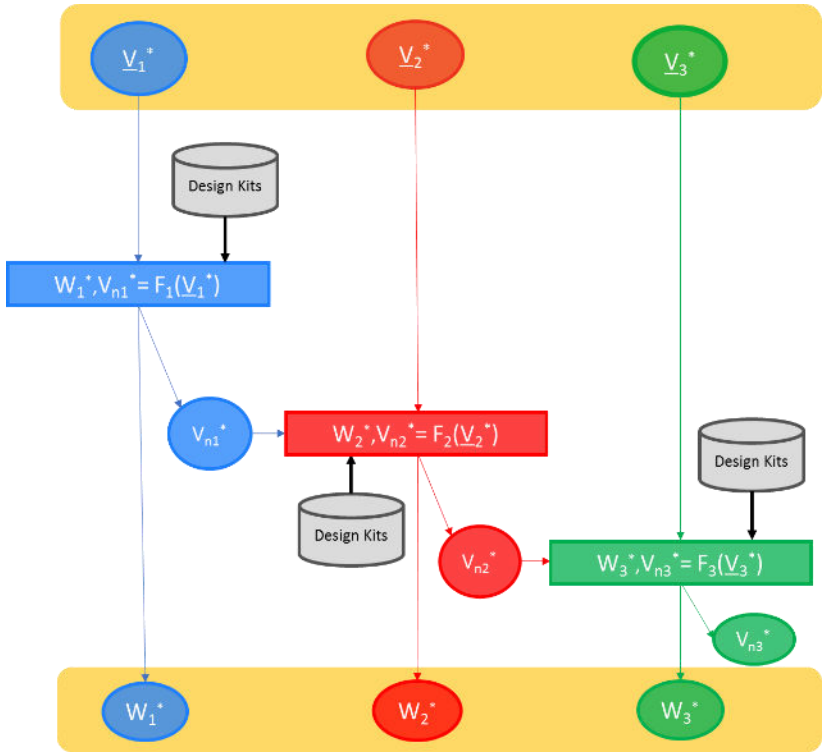

Fast, Error-Free, Deterministic and Correct-by-Construction

ID-Xplore™

A Deterministic AI Knowledge Graph Solver for Analog Chip Design and Migration

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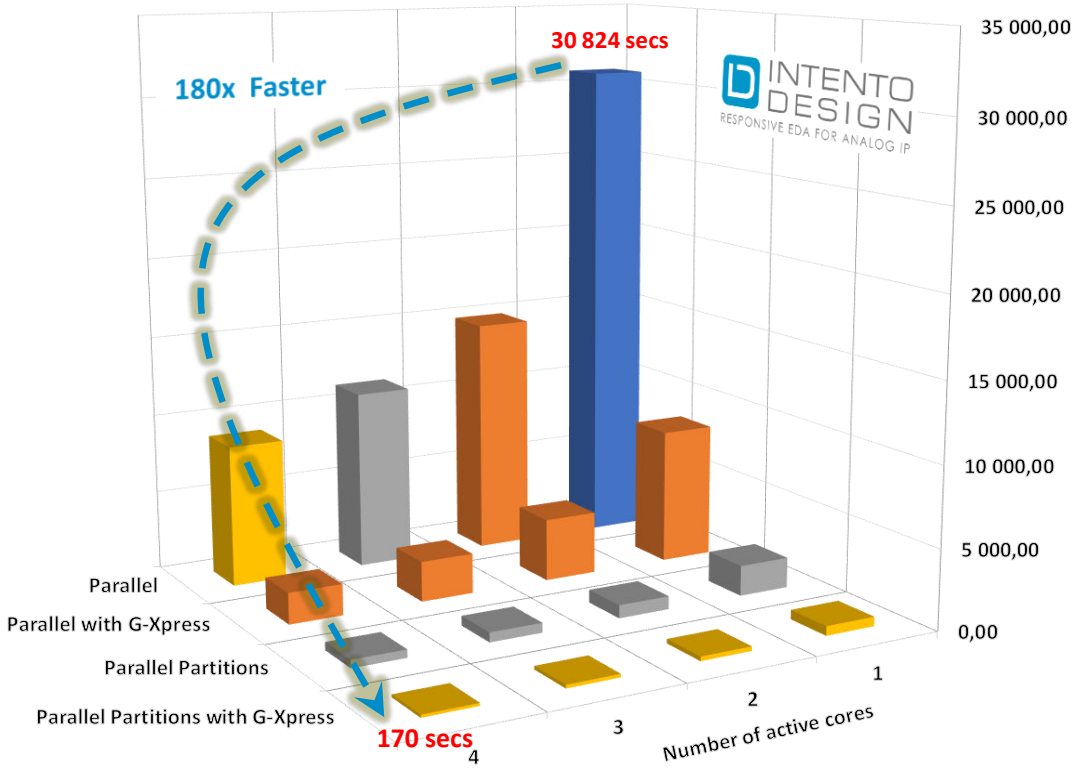
Use Case: Sizing a 75-Devices Class AB RF-Amplifier



Ultra Fast Design & Migration thanks to:

- Jacobian Free computations
- Graph-Based Model of Computation
- Graph-based Design Approach
- Intelligent Design Space Partitioning
- Intelligent Design Space Exploration
- Using multi-core and Compute Farm
- Very Fast Graph-Based PVT Analysis

Analog Design Flow with ID-Xplore™

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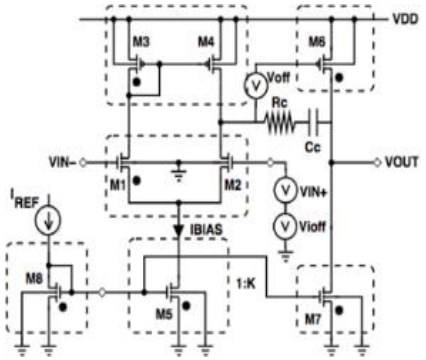
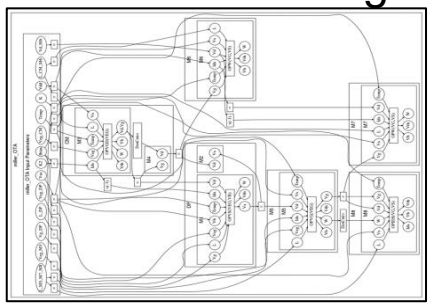
XPLORE

Schematic Entry

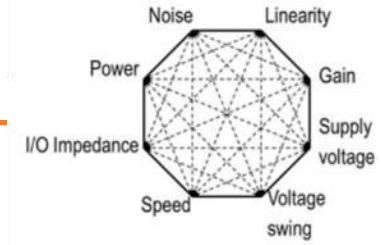


DC Bias & Transistor Sizing



Analog DC Knowledge Graph Solver

PDK



Test Bench Schematic

Performance Specification

Positioning ID-Xplore™ in Analog Design Flow

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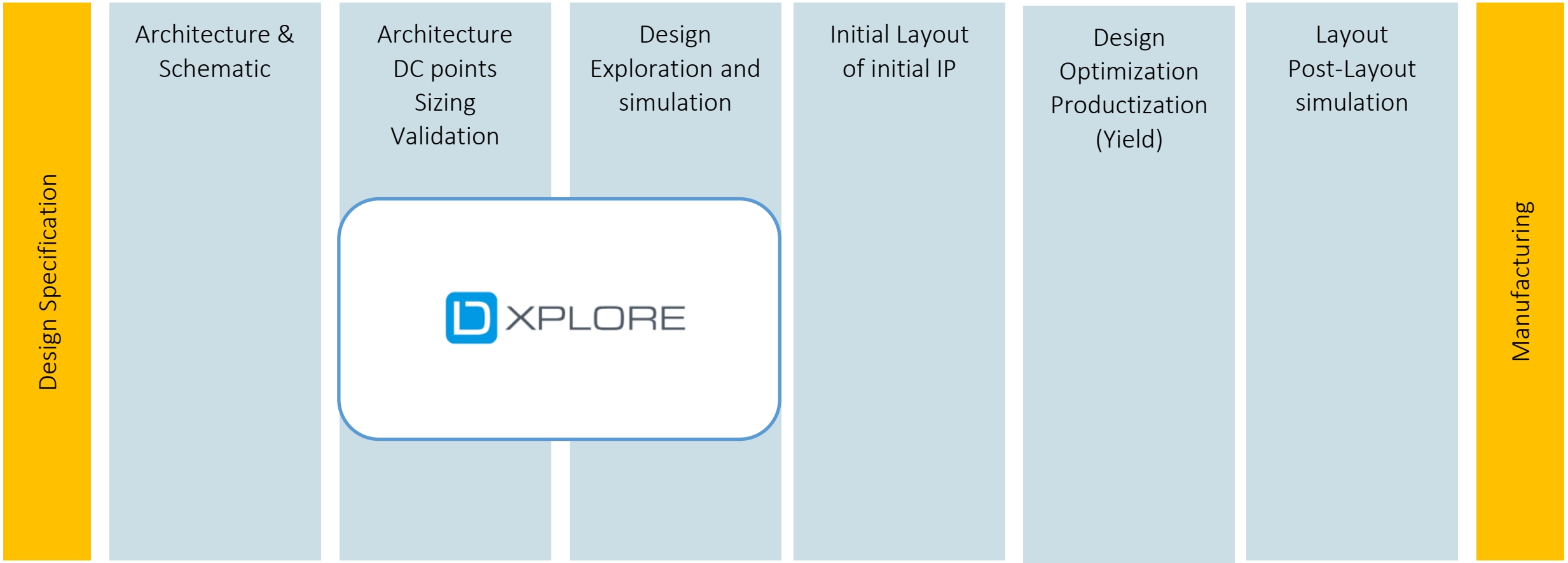
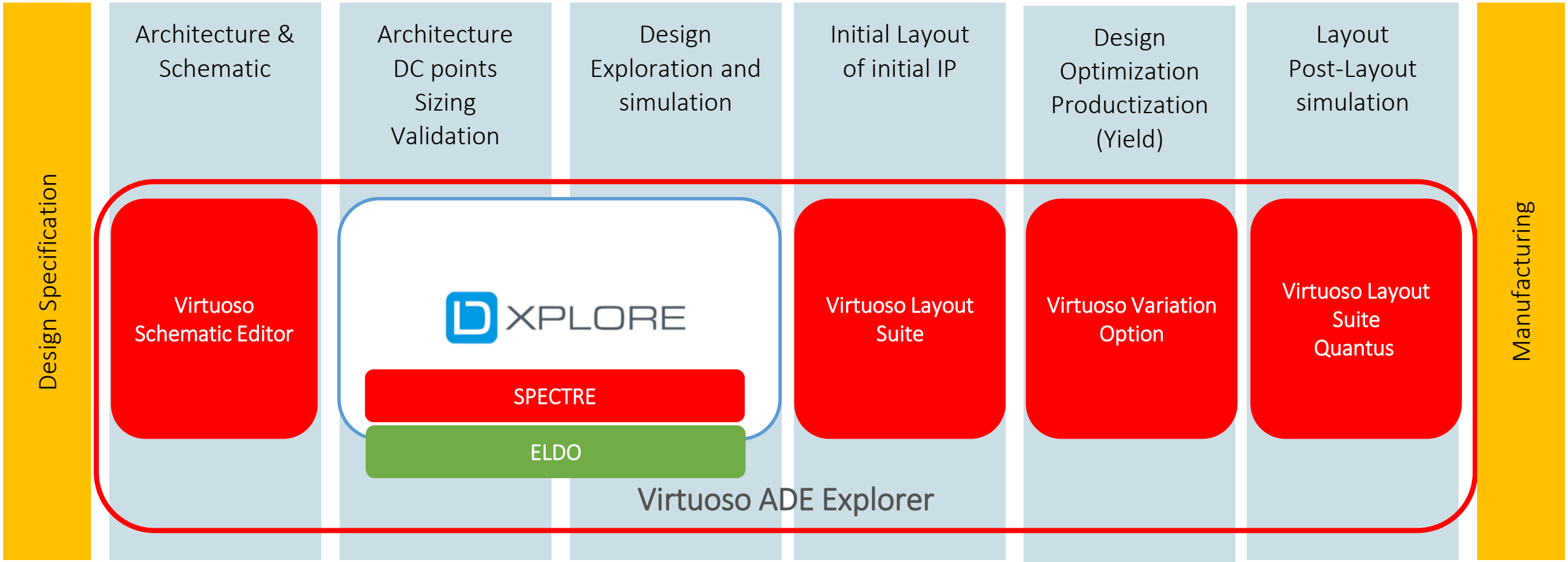
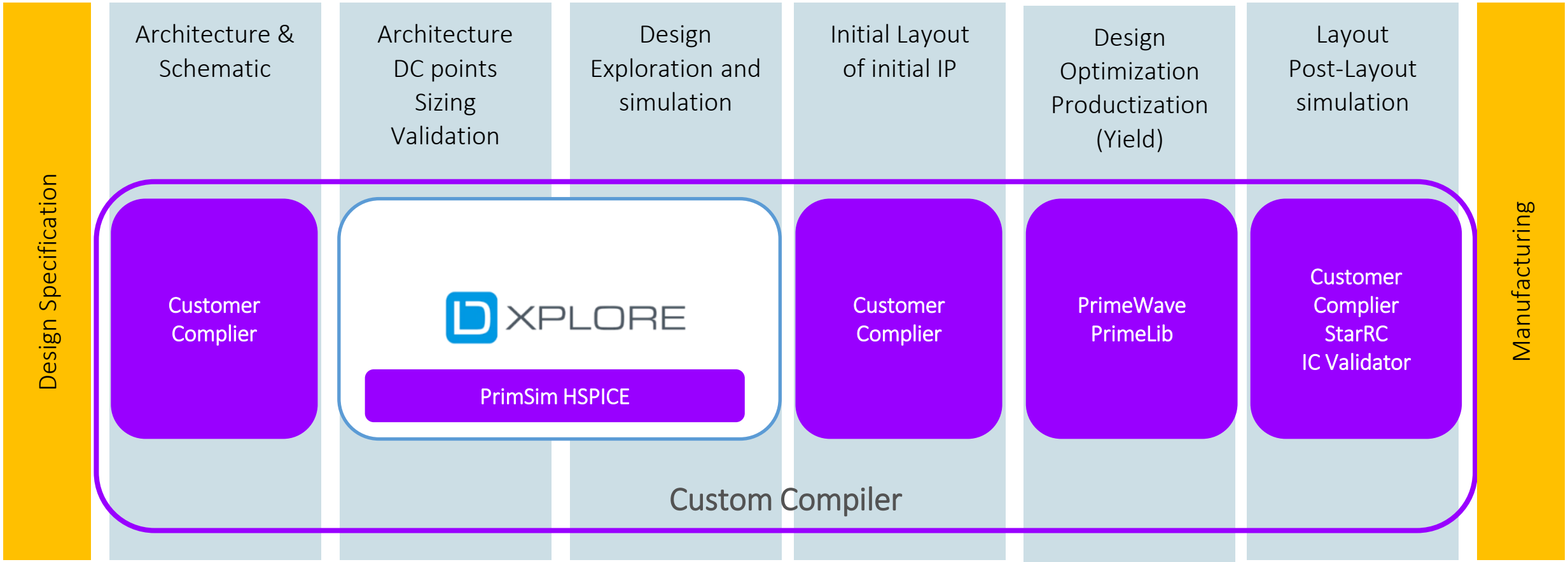


Positioning ID-Xplore™ in Cadence Analog Design Flow



Positioning ID-Xplore™ in Synopsys Analog Design Flow



XPLORE

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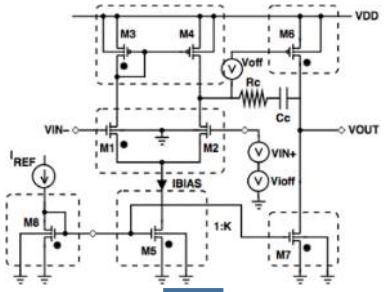
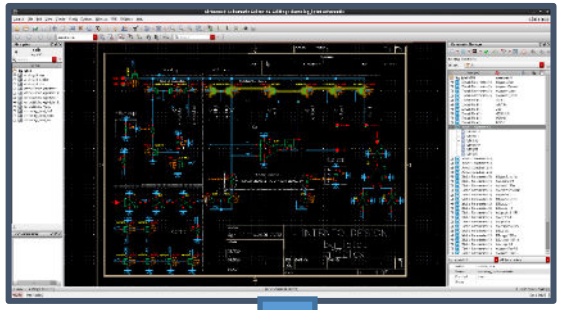
First Cognitive EDA for Design Exploration of Analog ICs

Unsized Schematic



Designer's Knowledge

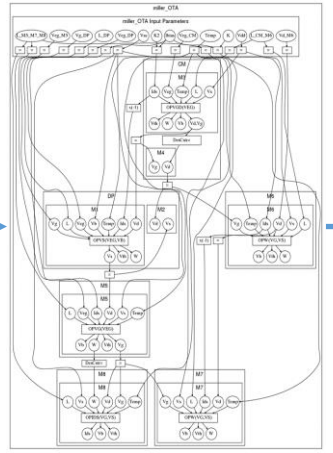
Electrical Parameters

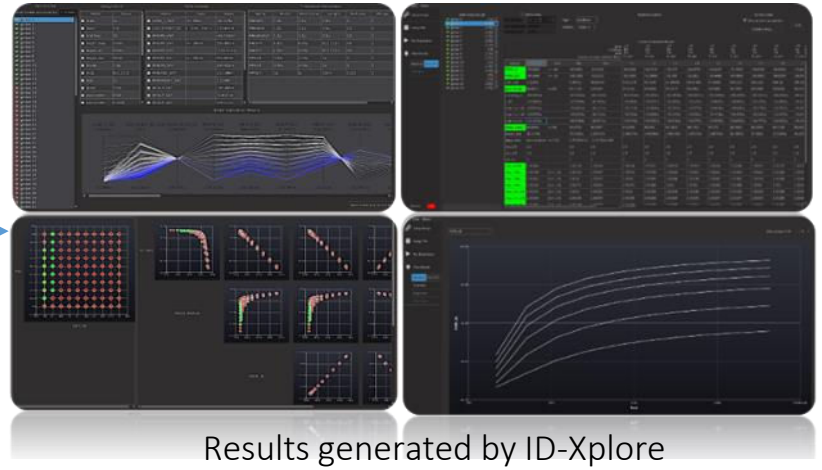


XPLORE

Knowledge Graph Solver

Structured Design Representation





Results generated by ID-Xplore

Added Values for Analog IC

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Customer

- Interactive top-down approach for analog designers (creativity + help Brainstorming ideas)
- Solution for tasks currently done outside computers
- Better use of analog experts time
- Quality focus & Start Validation upfront
- Efficient reuse & migration
- Build IP libraries
- High productivity gain

EDA Partner

- Introduce top-Down methdology in analog to gain and secure market share, based on top of existing products
- Differentiator with precise analog models
- Secure by patents
- Available products & team
- Important potential : RF, electrical checker, multi-domains, …
- High potential revenue

Under Development

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ID-VeriSpice™

Automatic Generation of Real Number Models for Analog IP

Why ID-VeriSpice™?

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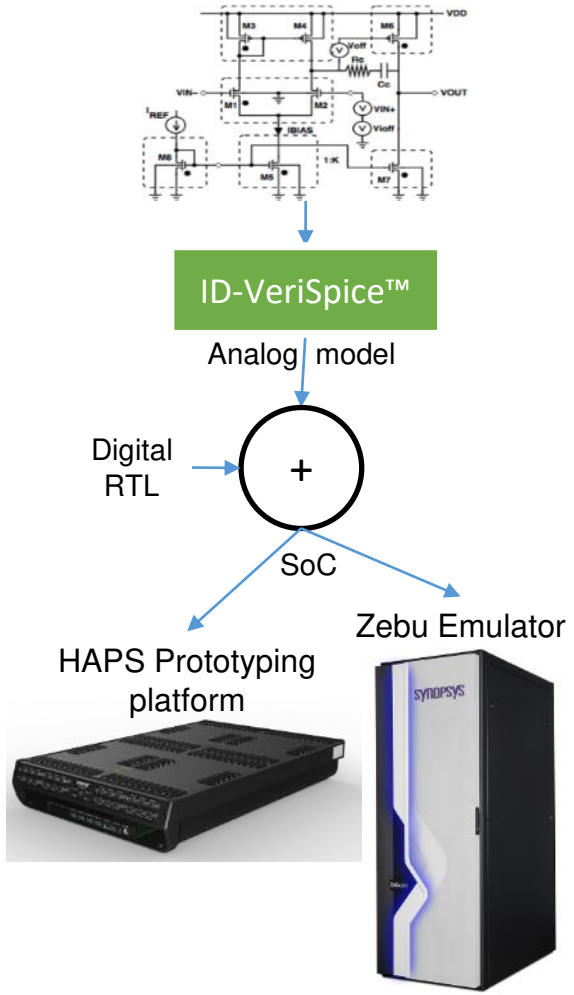
Concept:

- **Automatic conversion** of a **netlist/Schematic** of an **analog IP** into a **digital model** with **SPICE accuracy**

Use Cases

- **Verification** and **validation** of a **digital SoC** surrounded by **analog Ips**
- **Simulating** analog blocks in digital simulation environment with spice accuracy
- **Prototyping** of **SoC** and **system** including analog blocks (FPGA, HW-assisted system)
- System simulation for **reliability & failure analysis** (DFMEA/FMEA)
- Building comprehensive **Digital Twin** including **analog IPs** (PAVE 360, Twin Builder, …)
- **Transaction-Level modeling** for Analog Ips



Example : Full SoC-AMS Emulation

ID-VeriSpice™ Overview

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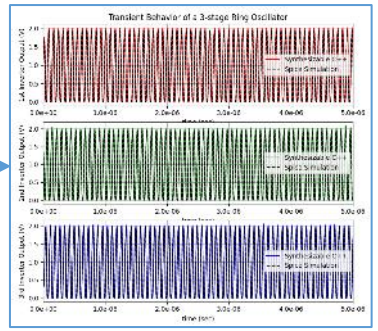
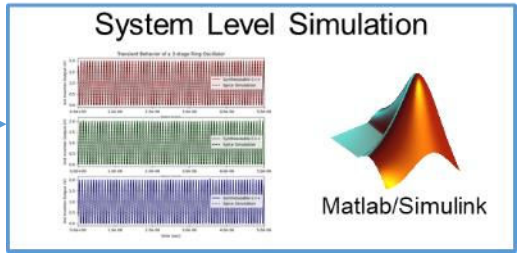
ID-VeriSpice™

.EXE
Generates all curves to verify the behavior of the model

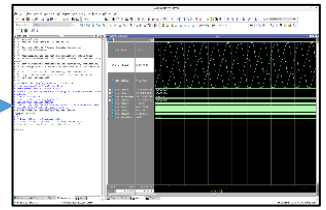


Model Verification
Used by Analog Designer to verify the behavior of the model before to deliver the model to the verification team.
Check if curves correspond to the analog simulation

Analog IP
C++ code



Digital Simulator (QuestaSim)



SoC Level Simulation / Verification

Analog IP
RTL code
(in Verilog)

RTL to FPGA

FPGA Prototyping

RTL to Emulator

HW Assisted Emulation

AMS Verification State-Of-The-Art

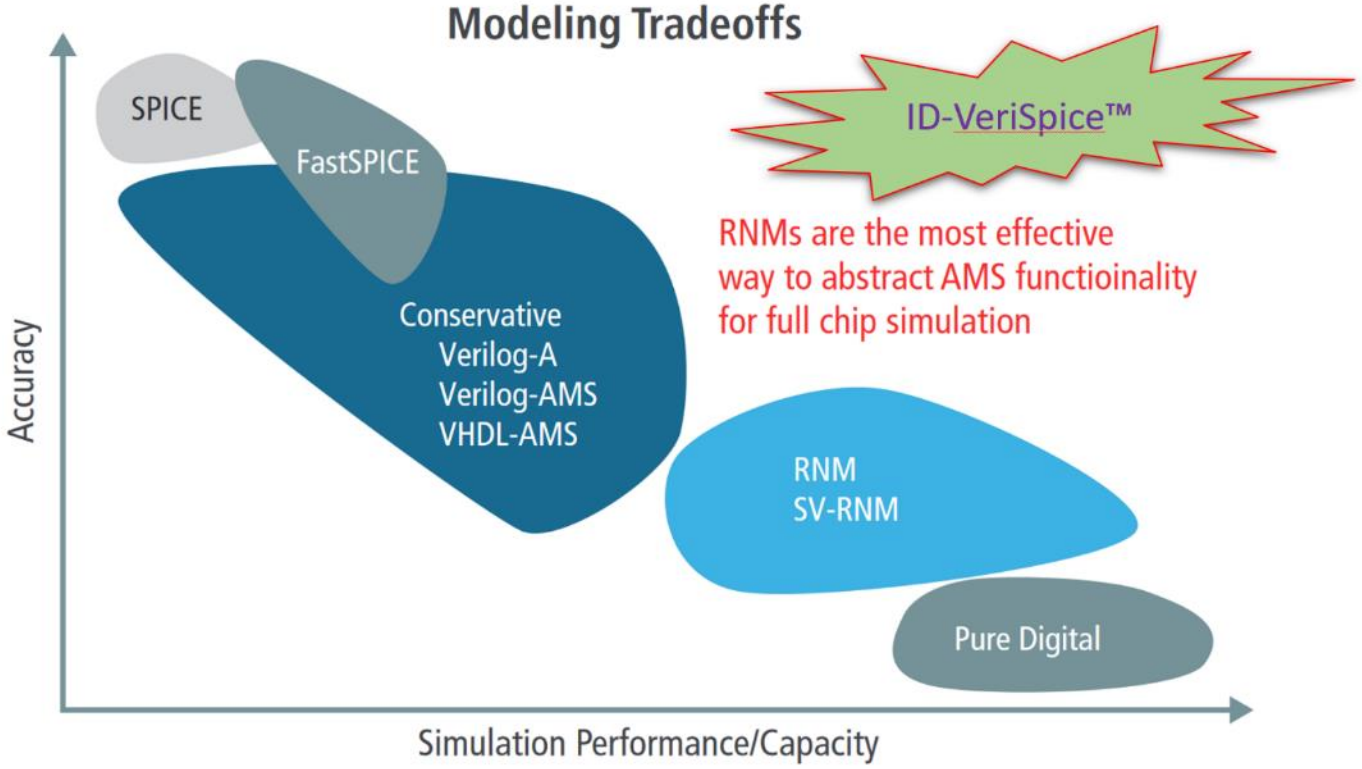


Figure 2: Model accuracy versus performance gain for mixed-signal simulation.

Limitation of Current AMS Modelling!

- Manual modelling in RNM
- No automation available
- Difficult to reach Spice accuracy
- Modelling depends on design expertise

ID-VeriSpice™ brings both Accuracy and Scalability

In Production

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ID-Substrate™ for Reliability

Verification and Signoff tool to ensure reliability and Robustness before tape-out

Why ID-Substrate™ ?

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ID-Substrate was developed to **predict and prevent substrate failures** quickly and accurately before the silicon fabrication

- **Minority carrier injection** and **lateral propagation** in substrate are difficult to model since they depend on layout distances.
- Existing SPICE simulators ignore the impact of these effects as they do **not look inside the substrate**.
- **Substrate failures** can therefore only be detected during lab tests after silicon is already fabricated and cause **circuit redesign**
- **40% of substrate failures** are due to minority carrier propagation.

ID-Substrate™ Value Proposition

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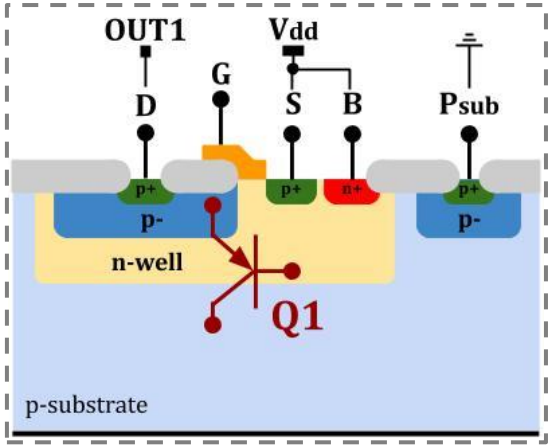
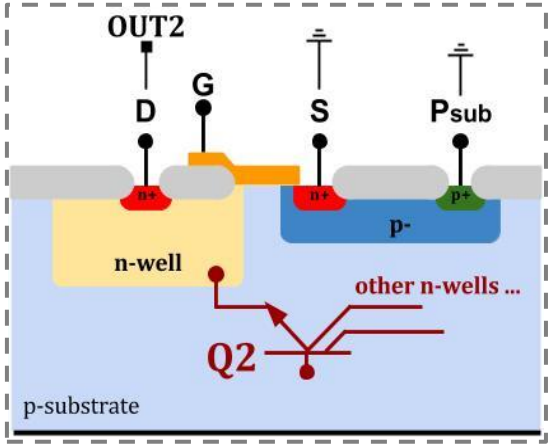
- Propose a modeling and simulation methodology for **systematic prediction and prevention** of substrate coupling effects and latch-up due to minority and majority carriers.
- Model multiple emitter/multiple collector **lateral bipolars**.
- Simulate complex substrate phenomena leading to **latch-up** conditions
- Simulate minority carrier propagation in **DC, AC & TRAN**.
- **CAD Framework** on top of OpenAccess Standard.
- A TCAD-Like behavioral **substrate simulation for full chip**





SUBSTRATE

A fast sign-off verification tool to capture and analyze all types of substrate noise coupling with high precision

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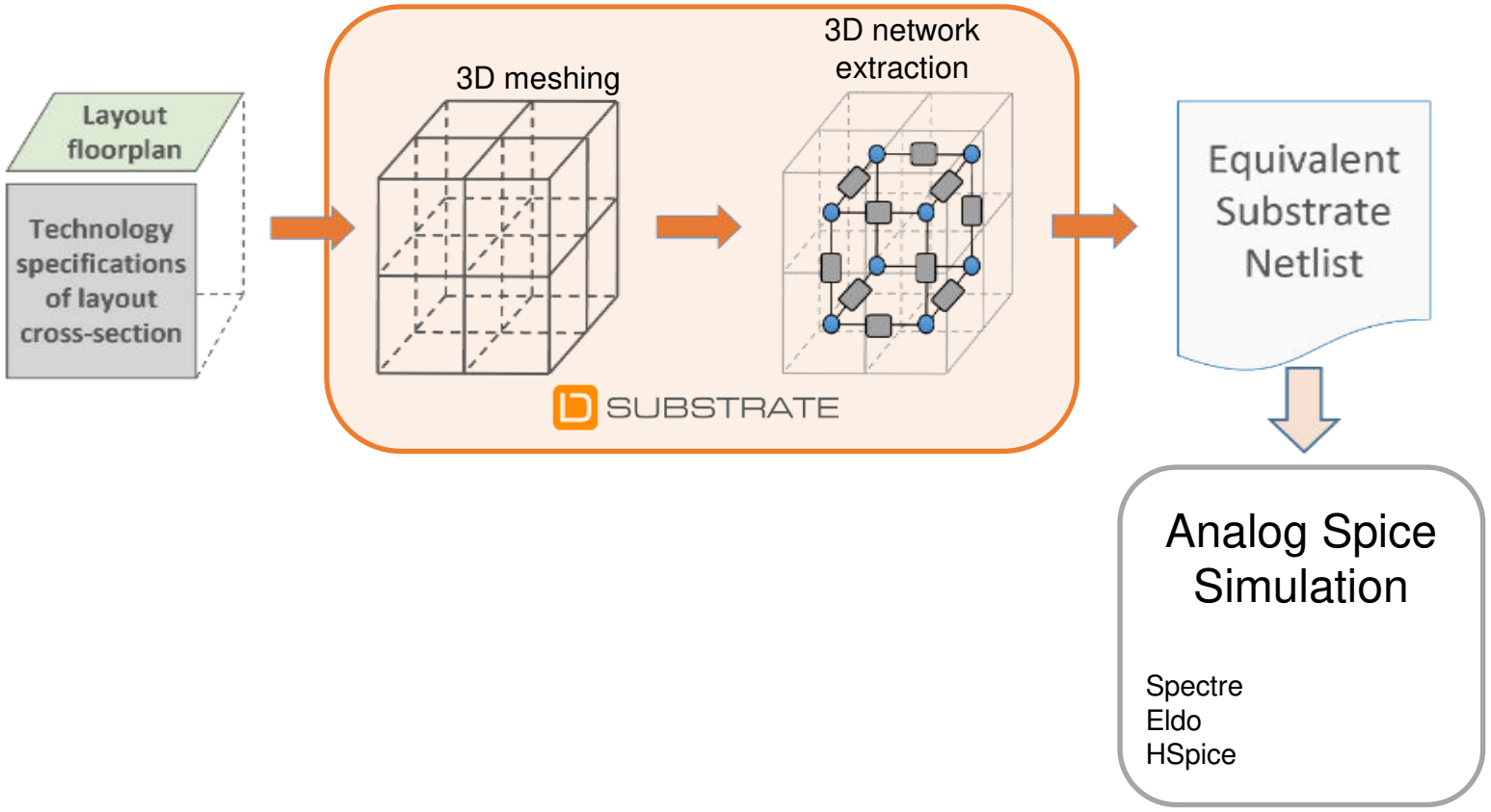
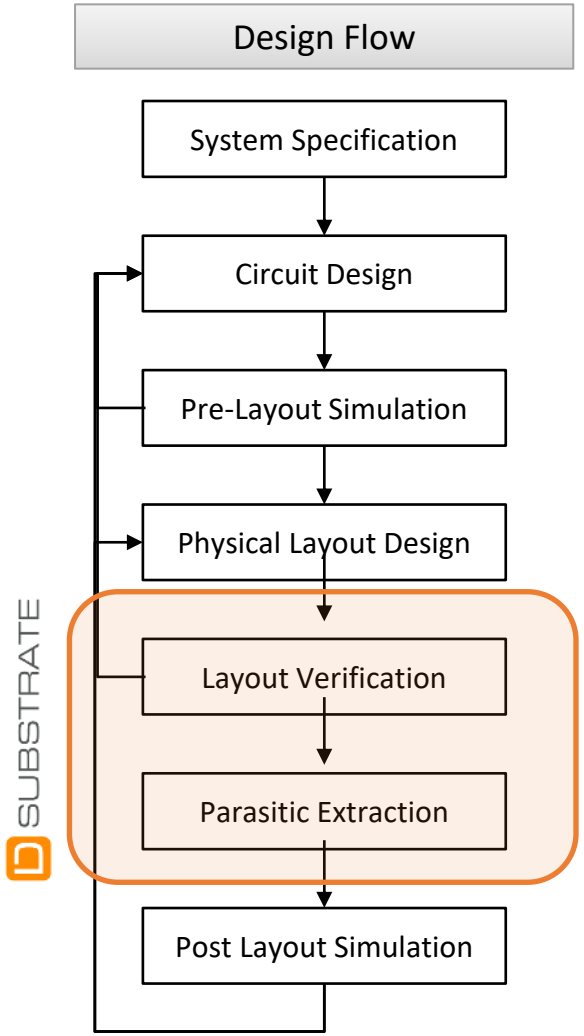
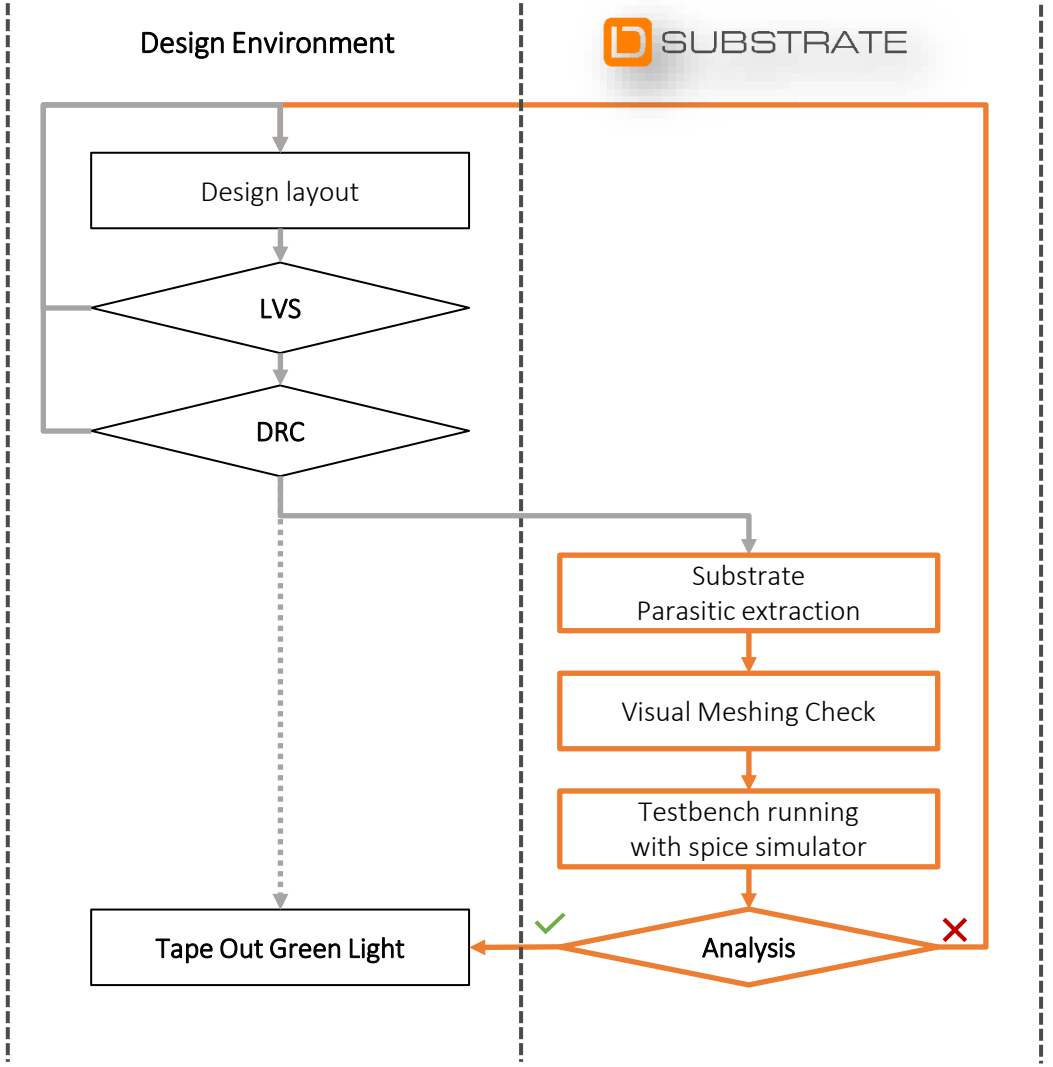
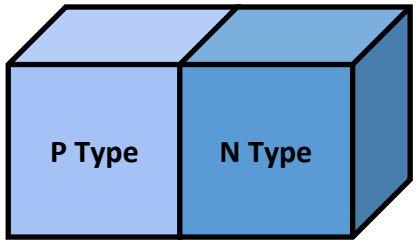


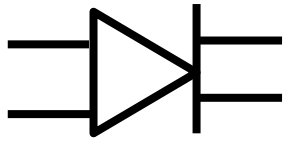


ID-Substrate™ Flow

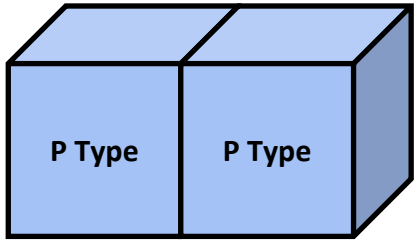


ID-Substrate™ Models

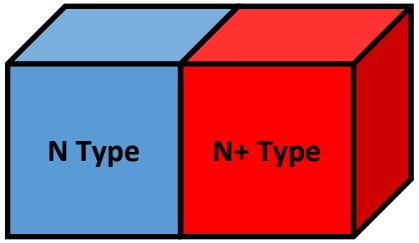




ID Diode



ID Resistor

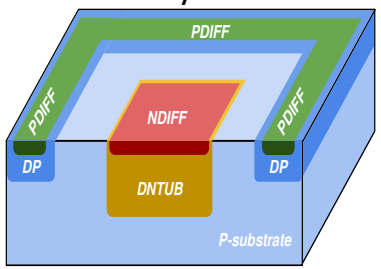


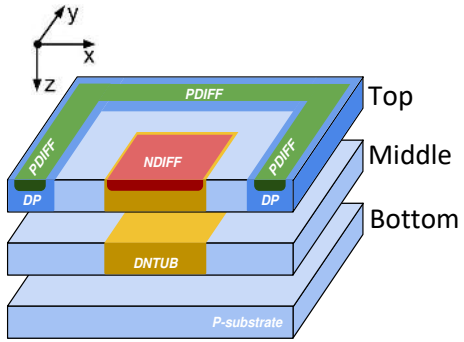
ID Homojunction

Meshing Strategy
Example with N-Well Diode in PSUB

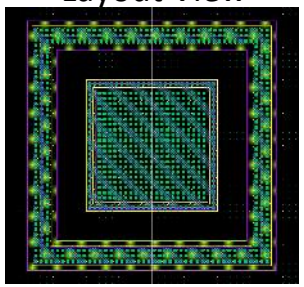
INTENTO DESIGN
INFORMED DECISION MAKING FOR ANALOG

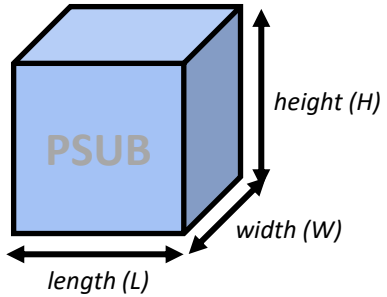
3D Layout View

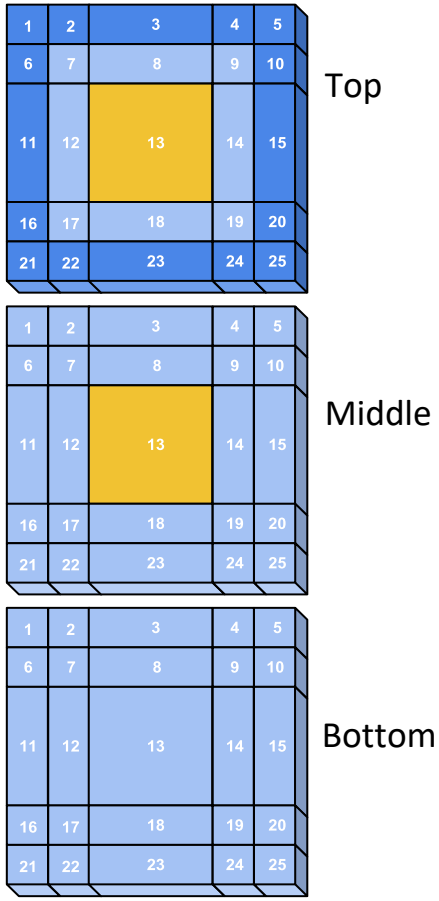


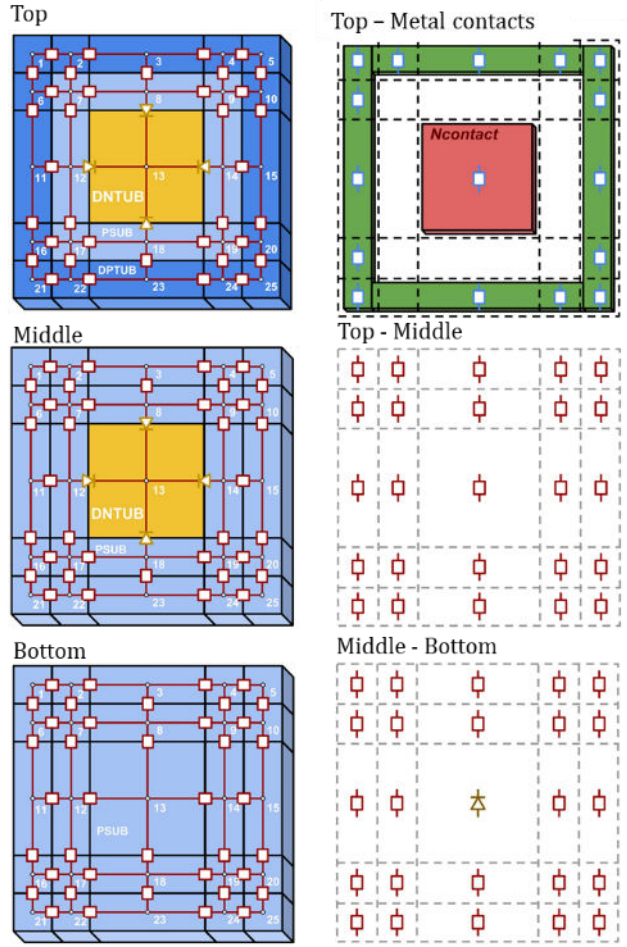


Layout View



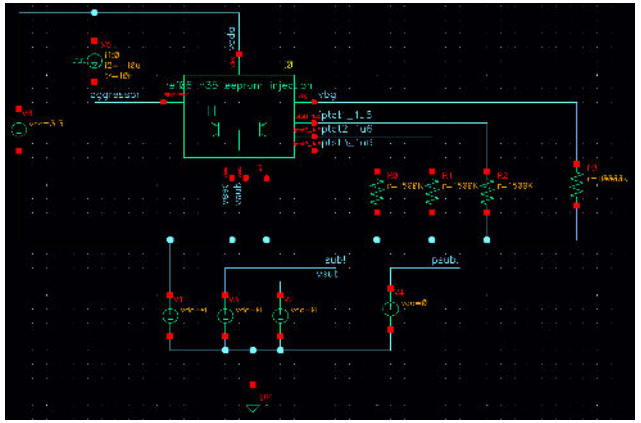


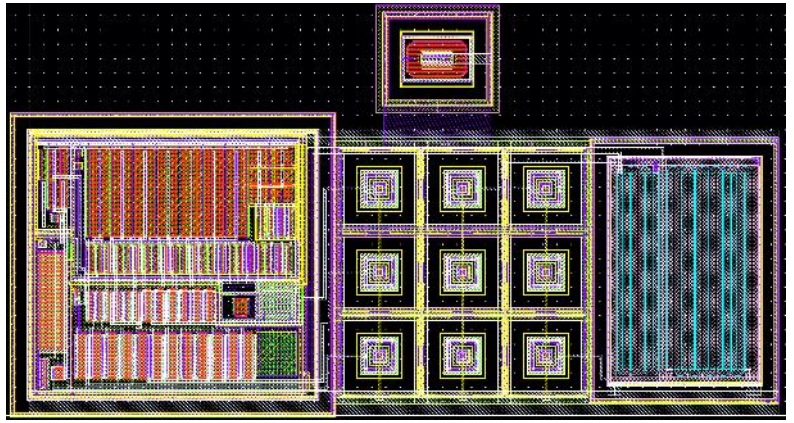




3D Substrate Network

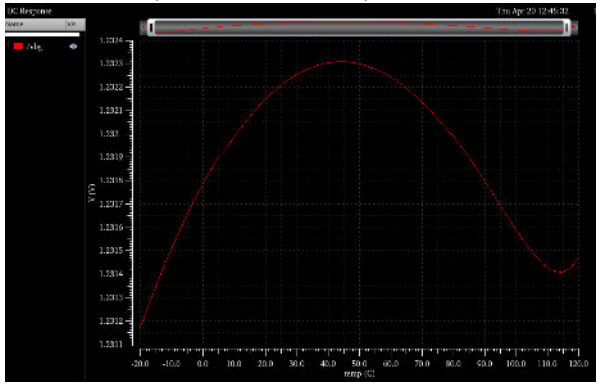
Substrate Coupling Detection
BandGap Simulation on AMS 0.35µm HV for Automotive





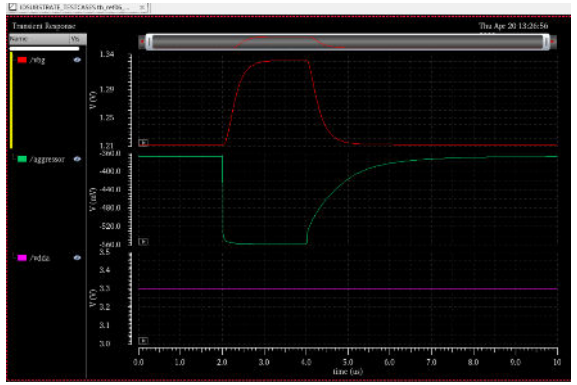
Transient Simulation

Temperature Compensation

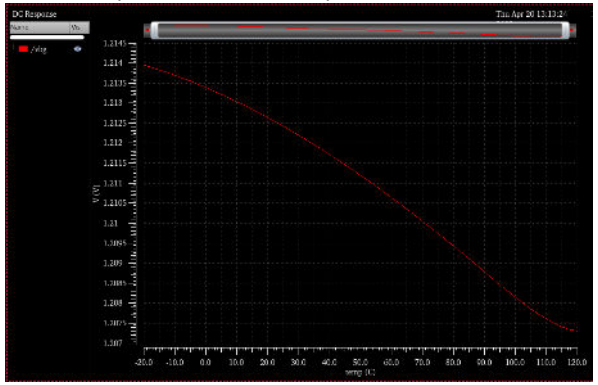


Without ID-Substrate Parasitic

Transient Simulation



Temperature Compensation

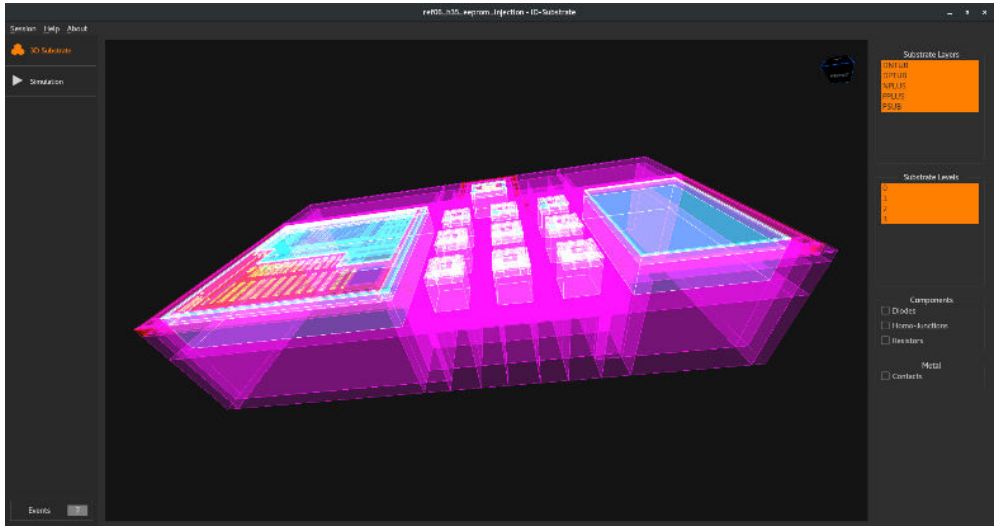


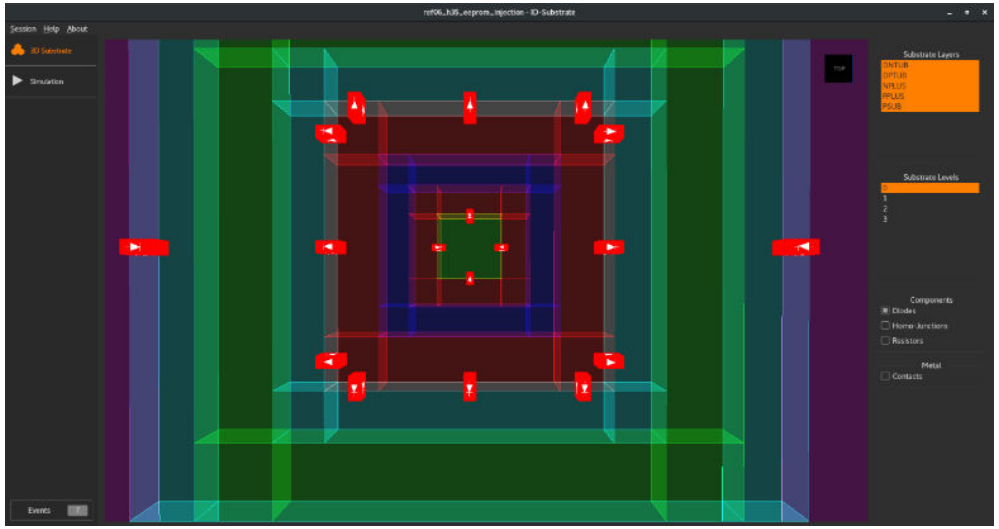
With ID-Substrate Parasitic

3D-Viewer for Substrate Parasitic (under development)

INTENTO DESIGN
INFORMED DECISION MAKING FOR ANALOG

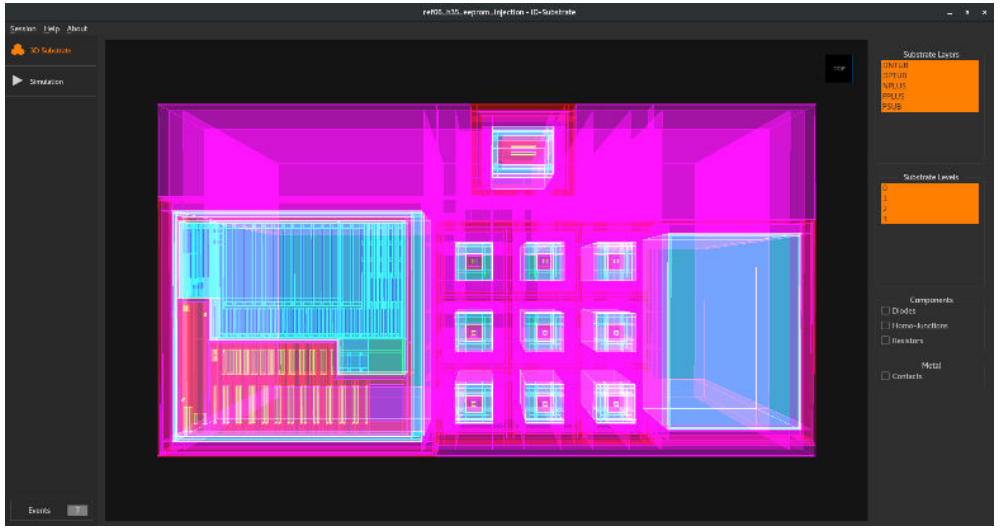
3D View

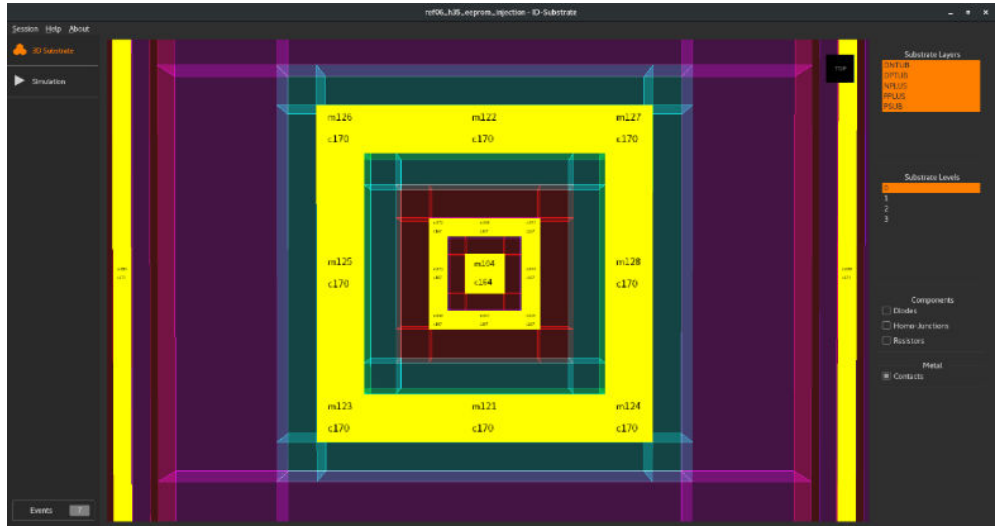




Diode Parasitic

Top View

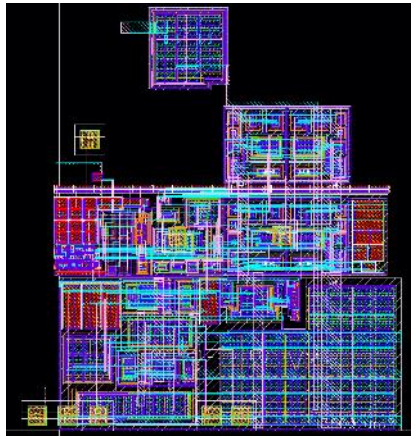




Substrate Contacts

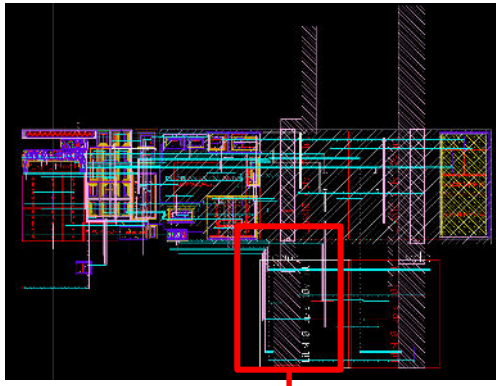
Static Identification of Latch-up Hotspots
No Simulation

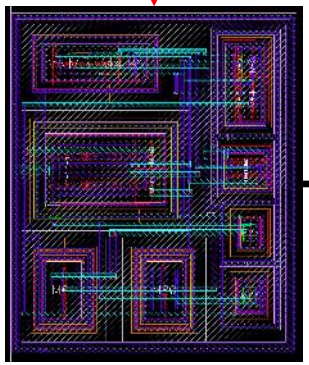
INTENTO DESIGN
INFORMED DECISION MAKING FOR ANALOG



Problem to solve:
Microcontroller with 2M devices with Latch-up issue.
Simulation for full chip not possible.

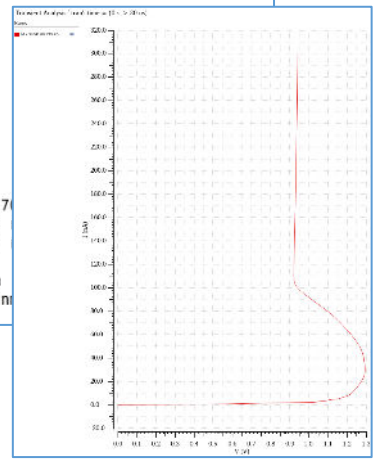
```
// ================================
// List of patterns: 18
// ================================
// Patterns number 1
// NPN para diode idx [514] and [510]
// Smallest NPN diode 1 idx: 71465, diode 2 idx: 70974
// PNP para diode idx [514] and [511]
// Smallest PNP diode 1 idx: 71465, diode 2 idx: 69424
// Box    : xmin: 34690, ymin: 23970, xmax: 40940, ymax: 76170
// Shapes :
// x: 35875, y: 25470
// x: 34690, y: 25470
// x: 34690, y: 23970
// x: 35875, y: 23970
// x: 35875, y: 25470
// ---
// x: 40940, y: 76170
// x: 34690, y: 76170
// x: 34690, y: 63780
// x: 35875, y: 63780
// x: 35875, y: 61605
// x: 40340, y: 61605
// x: 40340, y: 63780
// x: 40940, y: 63780
// x: 40940, y: 76170
// ---
// Path            : 2505,15234,15235,
// NPN Diodes, total: 7227, in range: all
// PNP Diodes, total: 2409, in range: all
// min distance     : 0 nm
// max distance     : 57939 nm
// average distance : 31986.8 nm
```





Hotspot Identification

```
// ================================
// List of patterns: 3
// ================================
// Patterns number 1
// NPN para diode idx [27] and [20]
// Smallest NPN diode 1 idx: 3466, diode 2 idx: 3471
// PNP para diode idx [27] and [10]
// Smallest PNP diode 1 idx: 3489, diode 2 idx: 3258
// Box    : xmin: 2810, ymin: 1310, xmax: 9710, ymax: 17070
// Shapes :
// x: 3870, y: 17070
// x: 2810, y: 17070
// x: 2810, y: 15510
// x: 3870, y: 15510
// x: 3870, y: 17070
// ---
// x: 9710, y: 12210
// x: 2810, y: 12210
// x: 2810, y: 2810
// x: 2810, y: 1310
// x: 3410, y: 1310
// x: 3410, y: 2810
// x: 9710, y: 2810
// x: 9710, y: 12210
// ---
// Path            : 145,280,7
// NPN Diodes, total: 5880, in
// PNP Diodes, total: 1740, in
// min distance     : 0 nm
// max distance     : 31982 nm
// average distance : 14703.2 n
```



Latch-up Triggering

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